Claims:

1. An apparatus comprising:

a memory element having one or more impermissible operations,

a plurality of memory access lines,

a code generator accepting a clock signal and generating a test code in response to said clock signal,

a decoder accepting said test code and generating at least two output lines where when in a decode enabled condition, said output lines are responsive to said test code and reflect a value on said output lines that when combined with respective memory access lines disables said one or more impermissible operations and when said decoder is in a decode disabled condition said output lines reflect a value that when combined with said respective memory access lines enables all possible memory operations.

2. An apparatus as recited in claim 1 wherein said code generator comprises a counter.

3. An apparatus as recited in claim 1 wherein said code generator comprises a random number generator.

4. An apparatus as recited in claim 1 wherein said memory element comprises a multiple port memory element.

5. An apparatus as recited in claim 1 wherein when in a decode enabled condition said decode circuit maps each test code value to a unique state of said output lines.

6. An apparatus as recited in claim 1 wherein when in a decode enable condition, said decode circuit maps more than one test code value to a state of said output lines.

7. A method for built in self test of a circuit including a memory element having one or more impermissible operations, said method comprising the steps of:

storing a seed value into a code generator,

generating a test code in response to a clock signal,

mapping said test code to at least two output lines,

combining respective ones of said output lines with a memory operation signal to generate a memory access enable signal, wherein when in a test code enabled condition, said step of mapping causes said output lines to reflect values that when performing the step of combining, the resulting said memory access enable signals disable said one or more impermissible operations and when in a test code disabled condition, said step of mapping causes said output lines to reflect values that when performing the step of combining, the resulting said memory access enable signals permit all possible memory operations without intervention, and

accessing the memory element.

8. A method for built in self test of a circuit as recited in claim 7 wherein said step of generating a test code comprises the step of generating a random number as said test code.

9. A method for built in self test of a circuit as recited in claim 7 wherein said step of generating a test code comprises the step of sequential number generation as said test code.

10. A method for built in self test of a circuit as recited in claim 7 and further comprising the step of driving all output lines to a positive value when in a test code disable condition.

11. A method for built in self test of a circuit as recited in claim 7 wherein the step of mapping further comprises mapping each test code value to a unique state of said output lines.

12. A method for built in self test of a circuit as recited in claim 7 wherein the step of mapping further comprising mapping more than one test code value to a single state of said output lines.

13. An apparatus for built in self test of a printed circuit board comprising:

at least one logic circuit,

at least one memory element having one or more impermissible operations,

a plurality of memory access lines for each memory element,

a code generator for each memory element accepting a clock signal and generating a test code for each memory element in response to said clock signal,

a decoder for each memory element, each decoder accepting said test code and generating at least two output lines for each memory element where when in a decode enabled condition, said output lines are responsive to said test code and reflect a value that when combined with respective memory access lines disables said one or more impermissible operations and when in a decode disabled condition said output lines reflect a value that when combined with said respective memory access lines enables all possible memory operations.

14. An apparatus for built in self-test as recited in claim 13 wherein at least one of said code generators comprises a counter.

15. An apparatus for built in self-test as recited in claim 13 wherein said code generator comprises a random number generator.

16. An apparatus as recited in claim 13 wherein at least one of said memory elements comprises a multiple port memory element.

17. An apparatus as recited in claim 13 wherein when in a decode enabled condition, at least one of said decode circuits maps each test code value to a unique state of said output lines.

18. An apparatus as recited in claim 13 wherein when in a decode enable condition, at least one of said decode circuits maps more than one test code value to a state of said output lines.

19. An apparatus as recited in claim 13 wherein all of said test code generators receive the same clock signal.

20. A method for built in self test of a printed circuit board including at least one logic circuit and at least one memory element comprising the steps of:
storing known seed values into a plurality of registers on the printed circuit board,
placing said printed circuit board in a test code enable condition,
storing seed values into at least one test code generator,
stimulating the printed circuit board with a clock signal,
generating a test code for each one of said at least one test code generators in response to a clock signal,
mapping each generated test code to at least two output lines where when in a test code enable condition, only one of said output lines reflects an active value during any one state,
conjunctively combining respect ones of said output lines with a memory operation signal to generate a memory access enable signal, and
accessing the memory element, and
comparing a resulting test signature with a known good test signature.

21. A method for built in self test of a printed circuit board as recited in claim 20 wherein said step of generating a test code comprises the step of generating a random number as said test code.

22. A method for built in self-test of a circuit as recited in claim 20 wherein said step of generating a test code comprises the step of sequential number generation as said test code.

23. A method for built in self test of a circuit as recited in claim 20 and further comprising the step of driving all output lines to a positive value when in a test code disable condition.

24. A method for built in self test of a circuit as recited in claim 20 wherein the step of mapping further comprises mapping each test code value to a unique state of said output lines.

25. A method for built in self test of a circuit as recited in claim 20 wherein the step of mapping further comprising mapping more than one test code value to a single state of said output lines.